# GPU Programming with CUDA

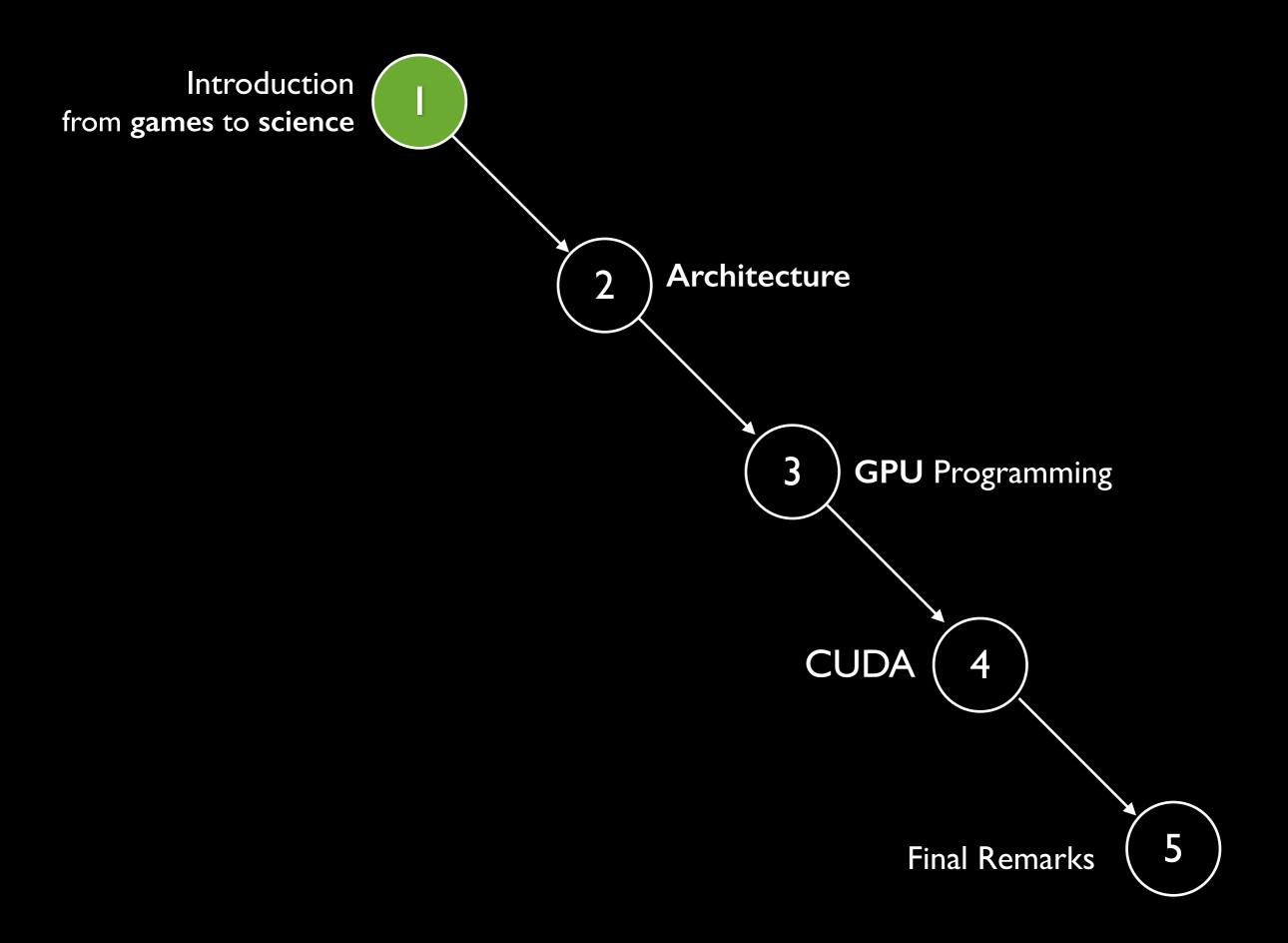
Pedro Velho

Meeting the audience!

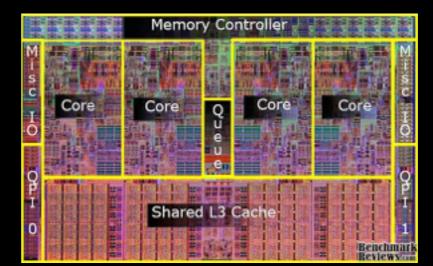
How many of you used concurrent programming before?

How many threads?

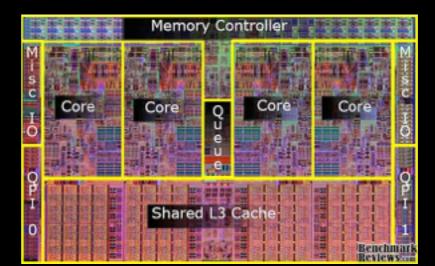
How many already used CUDA?



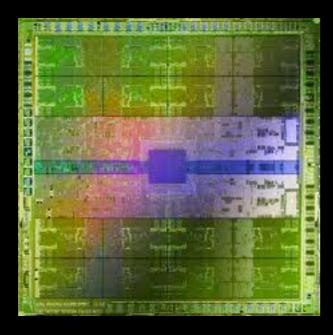
- A few general purpose cores
- -Big cache memory
- Eg.: Nehalem í7 quad-core
  - 4 cores (8 threads)
  - Cache is about 50% of die area



- A few general purpose cores
- Bíg cache memory
- Eg.: Nehalem í7 quad-core
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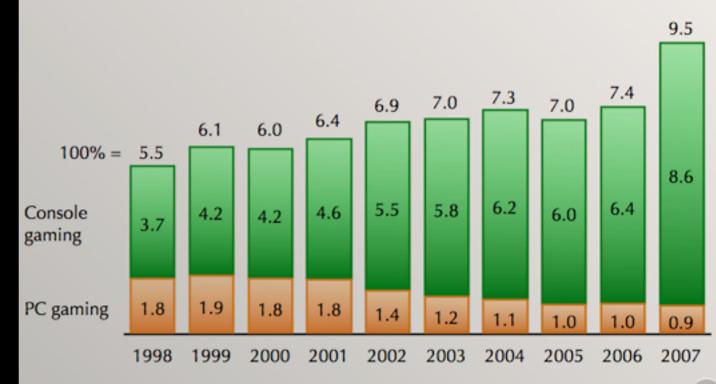
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- Design goal massívely parallel graphics
- A lot of replicated functional units
- Small cache síze
- Eg .: NVIDIA GTX280
  - 240 SP (streaming processors)
  - support for 30720 símultaneous threads

#### Computer Graphics is a Computational intensive application

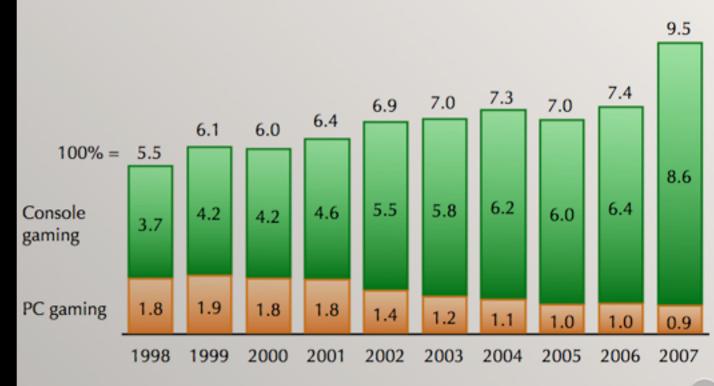
#### Video game software sales: 1998-2007 \$ Billions



#### Computer Graphics is a Computational intensive application

A lot of \$\$ from game industry

Video game software sales: 1998-2007 \$ Billions



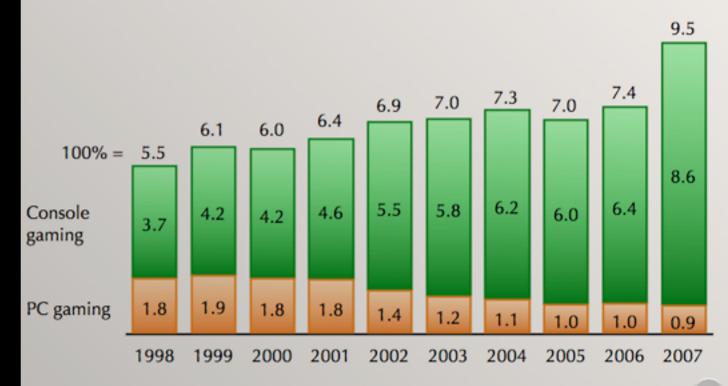
#### Computer Graphics is a Computational intensive application

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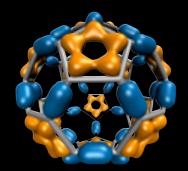
Expressíve gain in performance for parallel graphics rendering

Caught attention from the scientific community

Video game software sales: 1998-2007 \$ Billions



## GPU is also adapted to several scientific applications



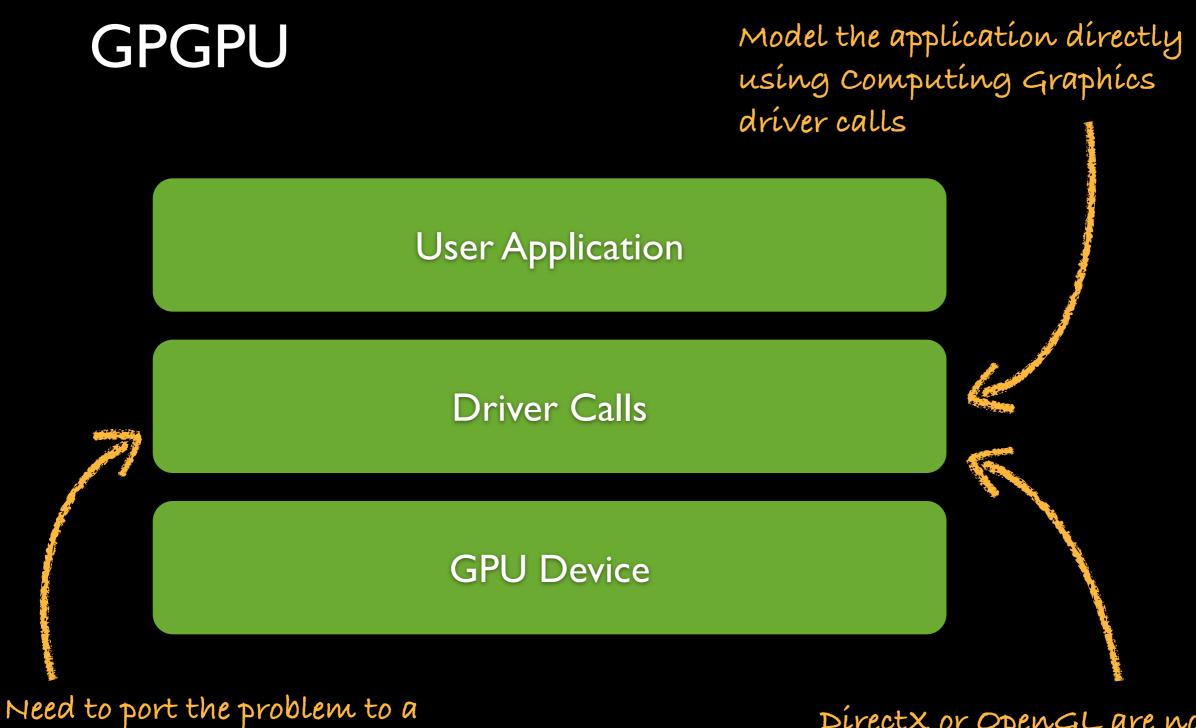




Molecular Biology

Fluid Simulation

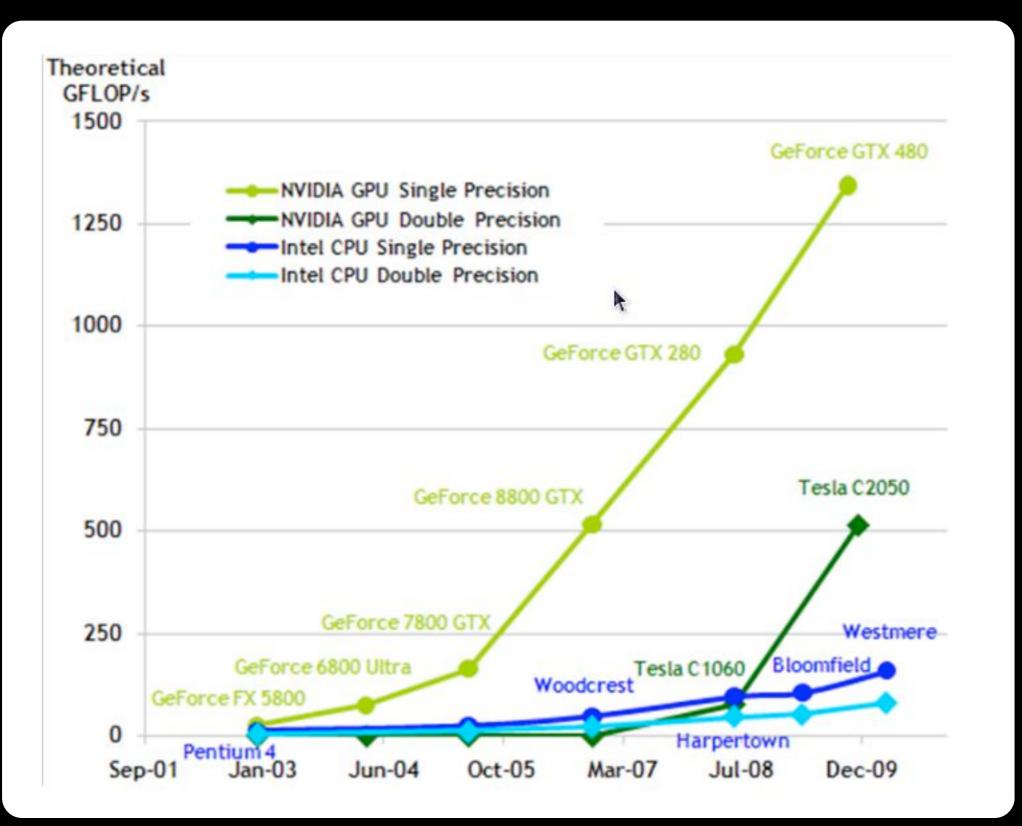
Weather Forecast



complete different domain

DírectX or OpenGL are not easy to figure out





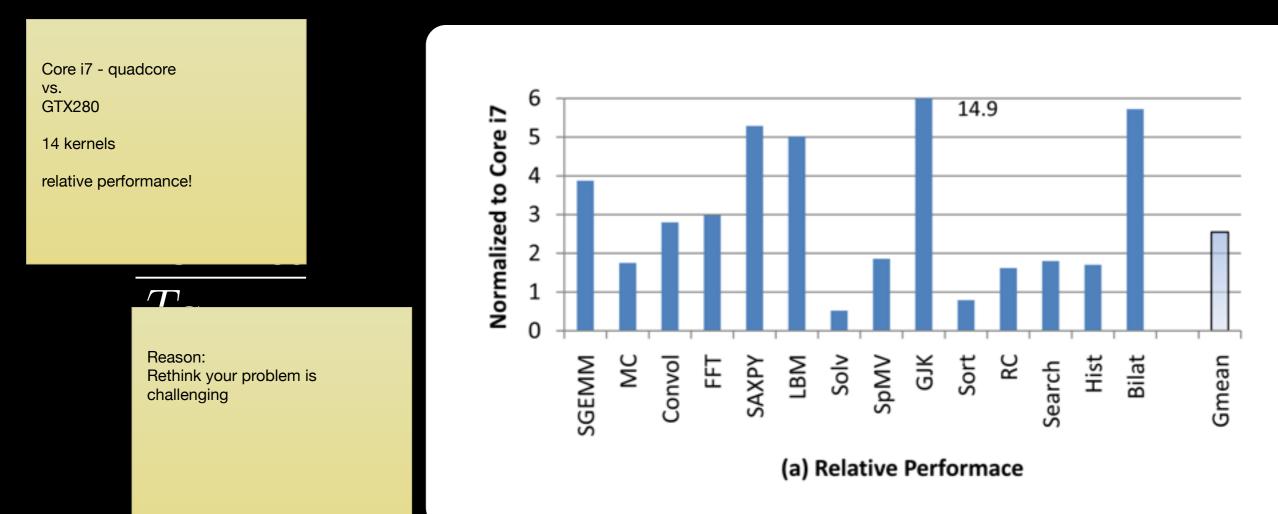
#### Potential Gain in Performance



Several guys from Intel

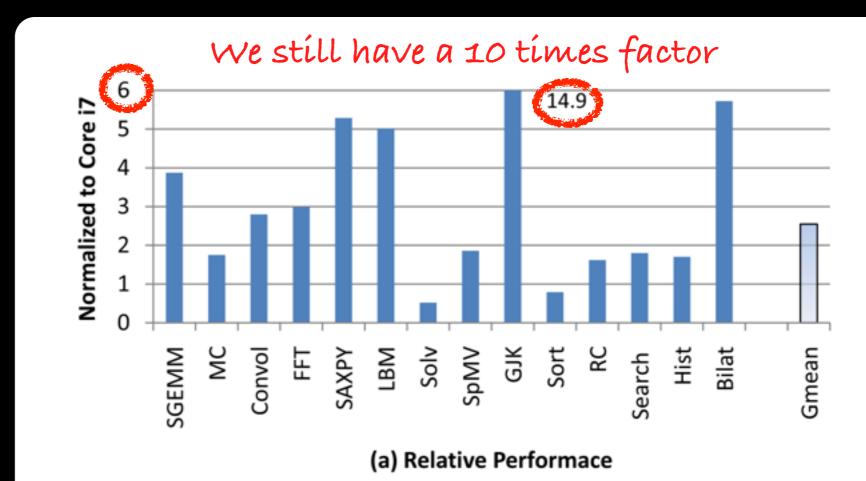


Victor W Lee et. al., Debunking the 100X GPU vs. CPU Myth: An Evaluation of Throughput Computing on CPU and GPU



### Potential Gain in Performance 100 times faster! Several guys from Intel This is a myth!

Victor W Lee *et. al.*, Debunking the 100X GPU vs. CPU Myth: An Evaluation of Throughput Computing on CPU and GPU



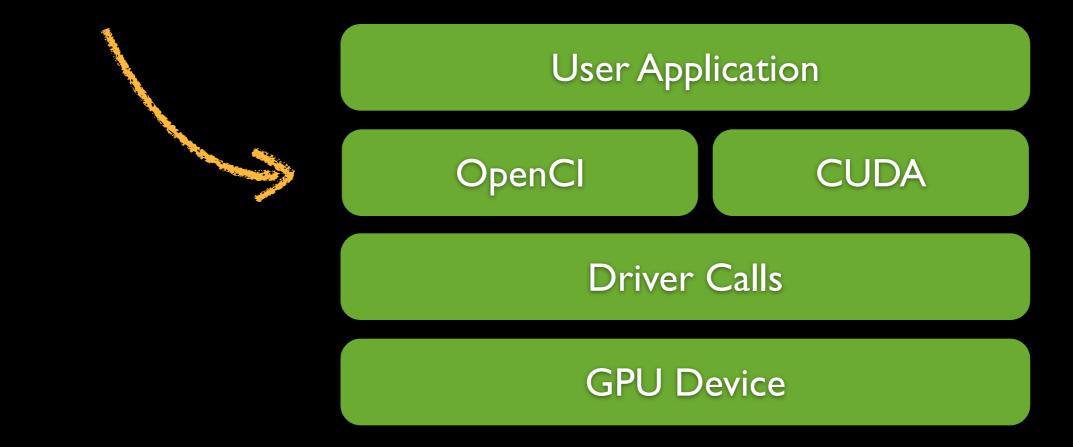
 $\frac{T_{\rm GTX280}}{T_{\rm Core~i7}}$ 

#### Substantial gain in execution time (10x)!

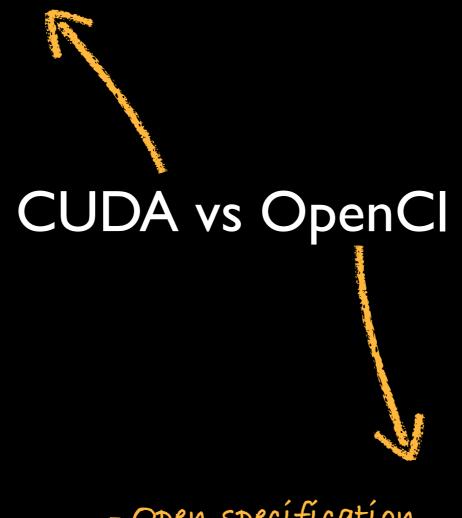
before GPU	with GPU	
one year	one month plus a week	
one day	two hours and twinty four minutes	
one hour	six minutes	

#### GPU Programming today

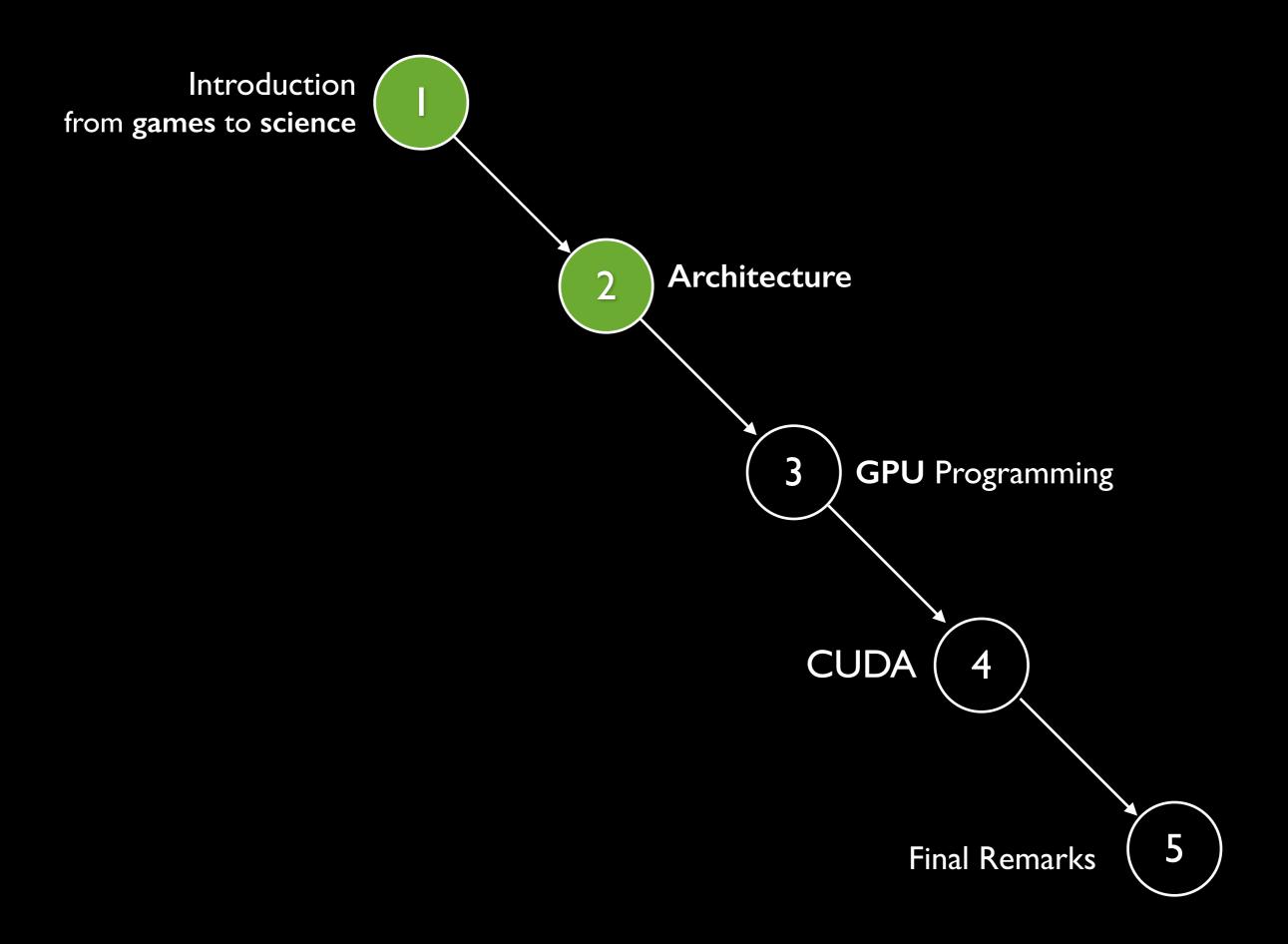
Don't need to port the application to DirectX or OpenGL



- Proprietary (only work on NVIDIA)
- Enhanced software support
- Several software libraries and examples

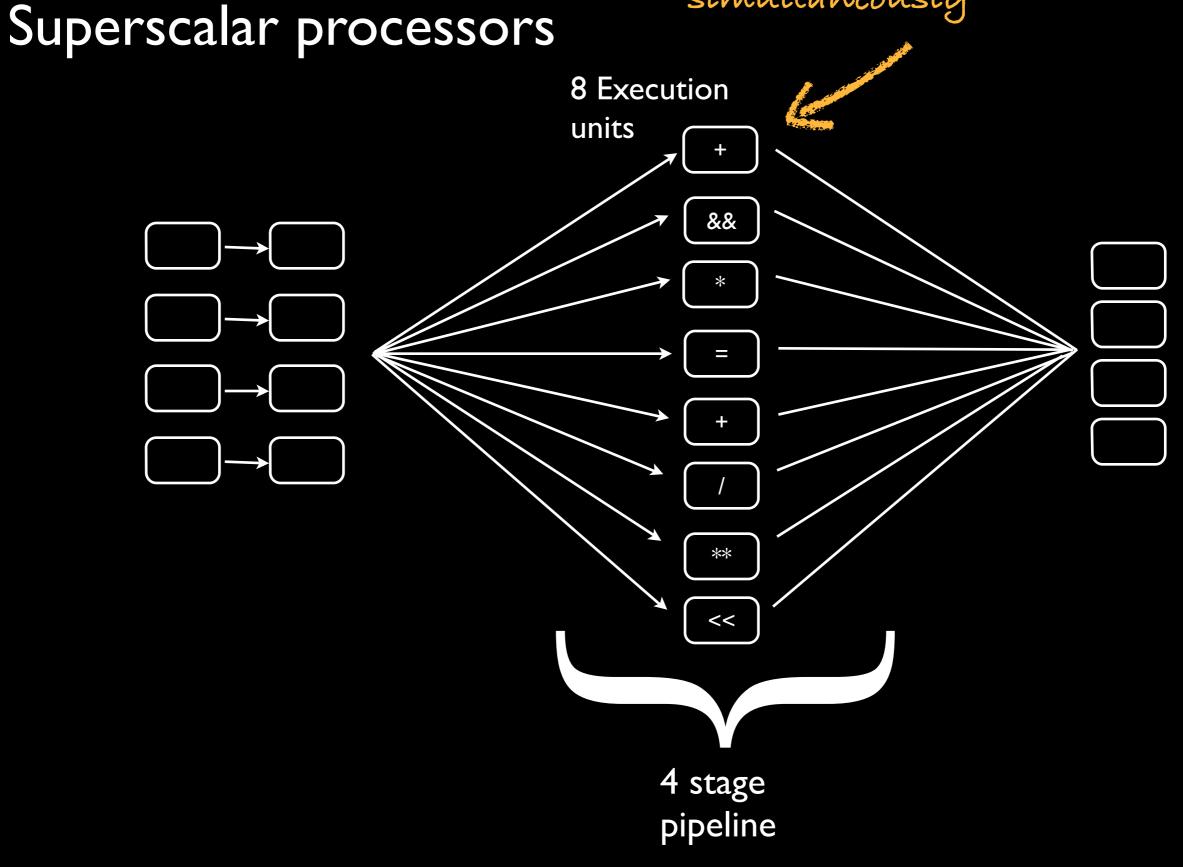


- Open specification
- Work on NVIDIA and ATI video cards
- Aim at any computing device



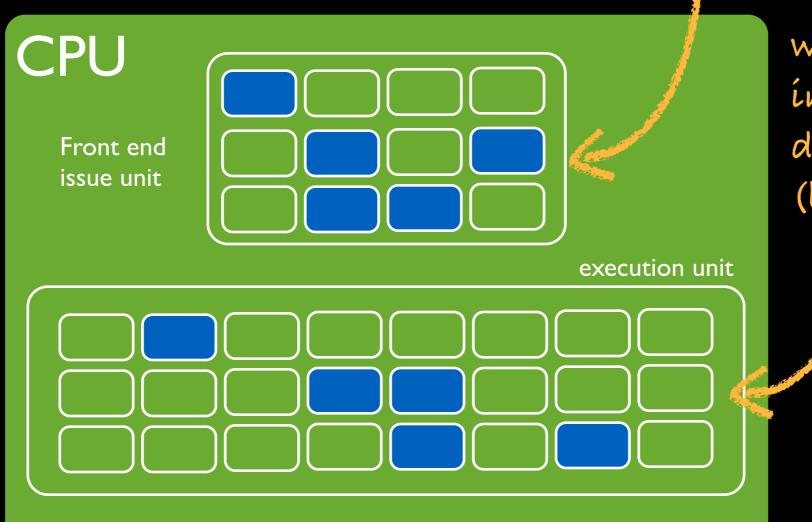
Computer Architectures from single thread to multithread

Execute up to 8 instructions simultaneously



### Superscalar processors make the illusion of concurrent execution

Instruction from one thread arrive A hardware íssue unít decídes whích ínstructíons can execute símultaneously

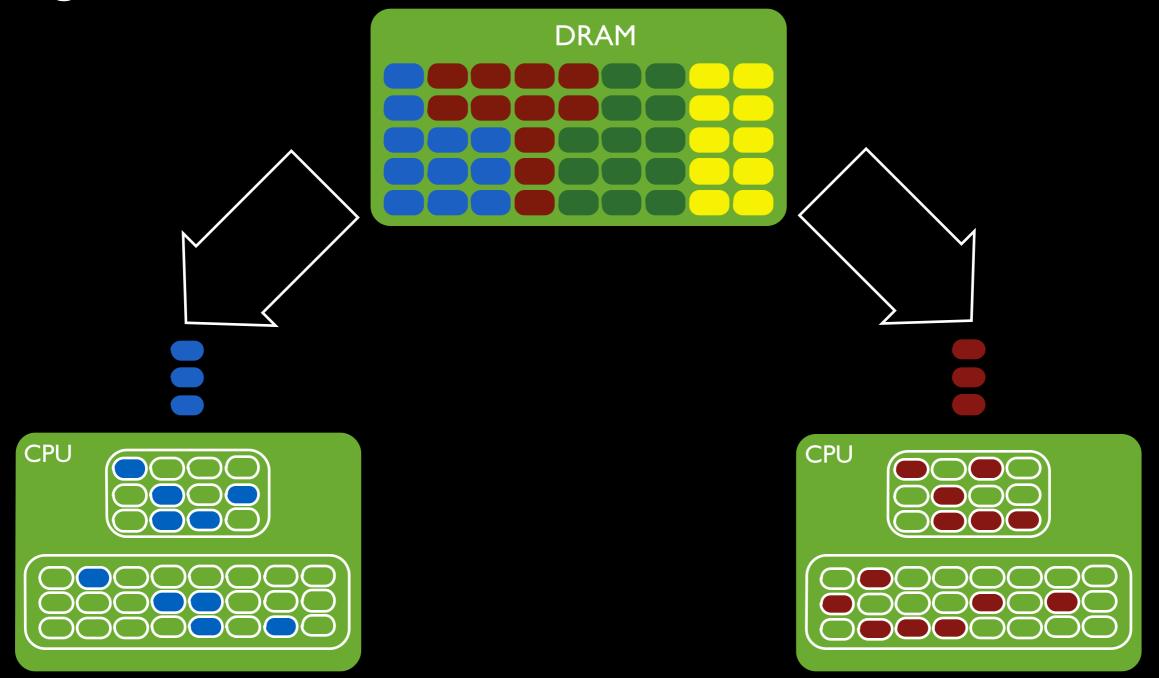


waste due to ínstruction dependecy (bubbles) A program has instructions for several threads in memory

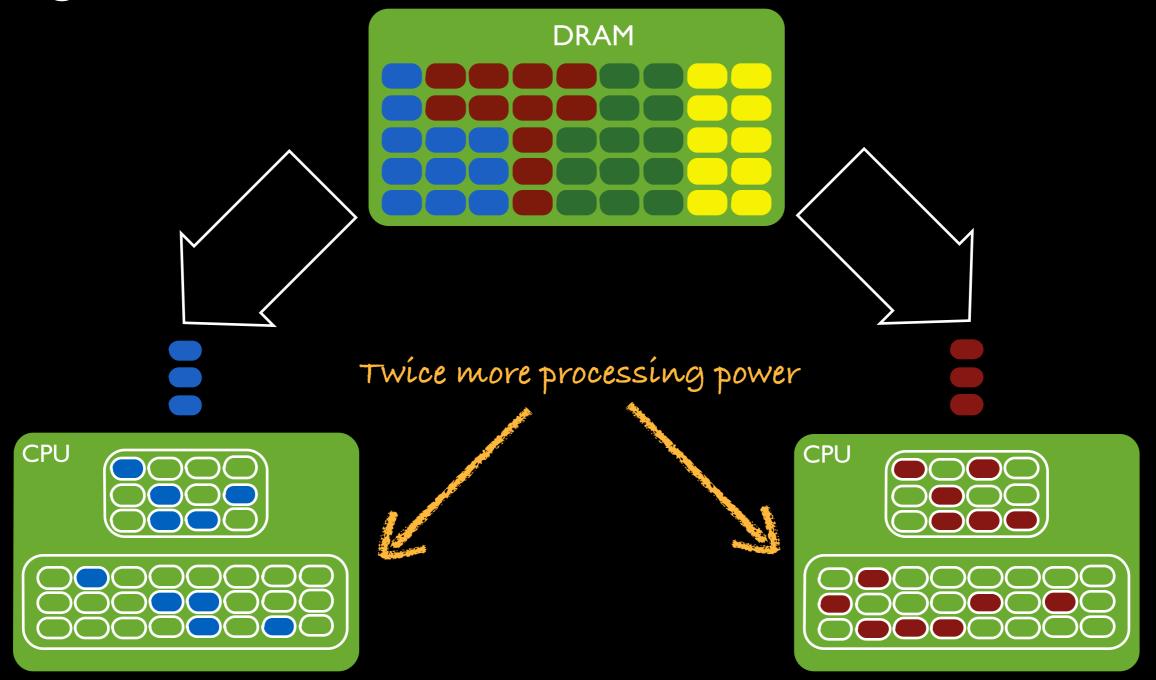


blue thread
red thread
green thread
yellow thread

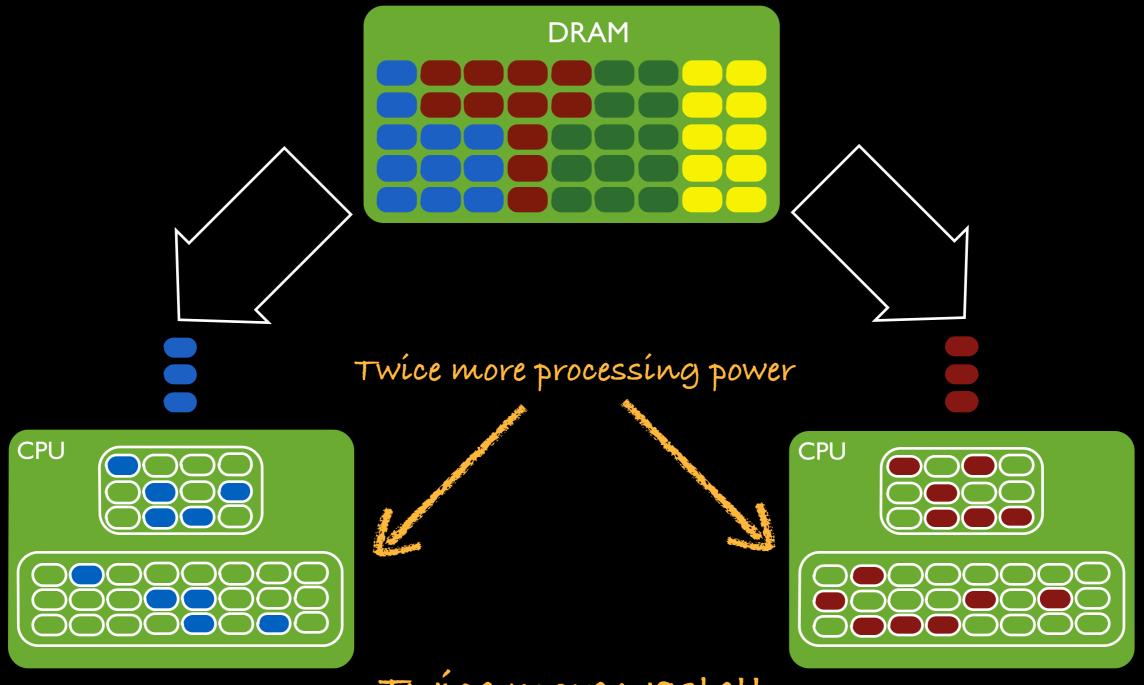
#### Single threaded multicore



#### Single threaded multicore

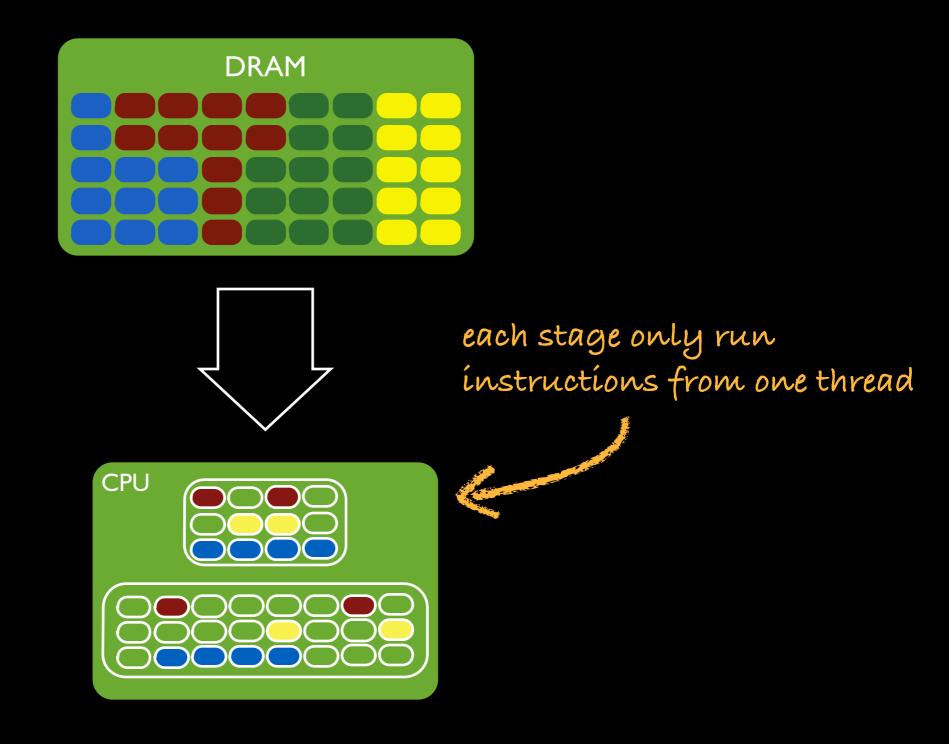


#### Single threaded multicore



Twice more waste!!

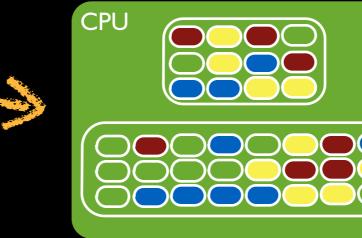
#### Super-threadeding



#### Multi-threadeding

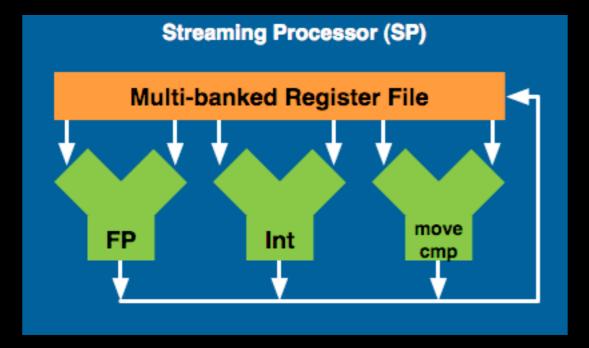


Execute instruction from more than 1 thread at a time

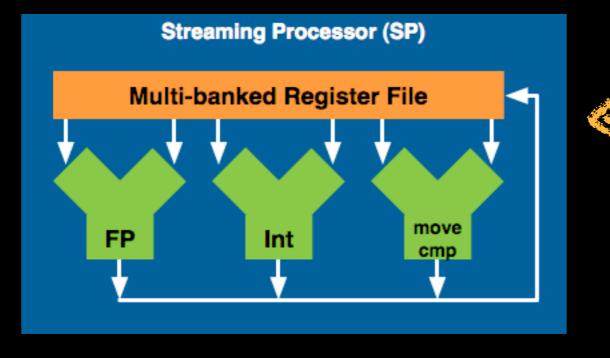


#### GPU architecture

#### Streaming Processor (SP)



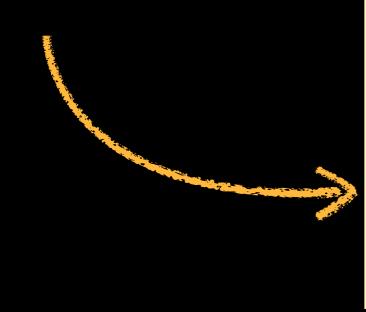
#### Streaming Processor (SP)

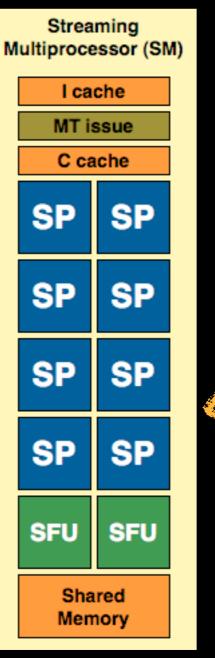


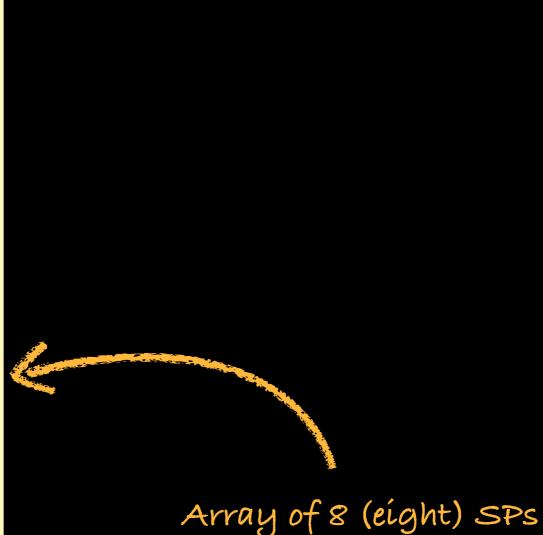


#### Streaming Multiprocessor (SM)

Each SFU 4 FP multíply for sín, cosín

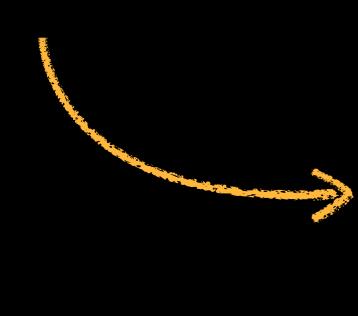


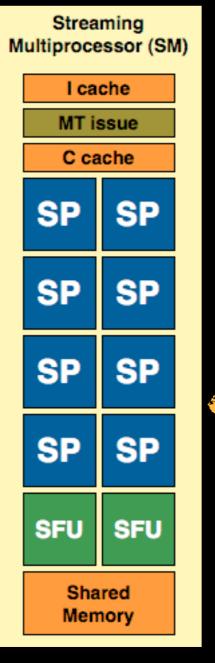


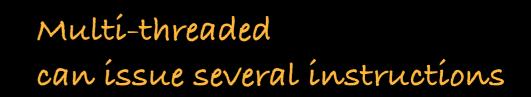


#### Streaming Multiprocessor (SM)

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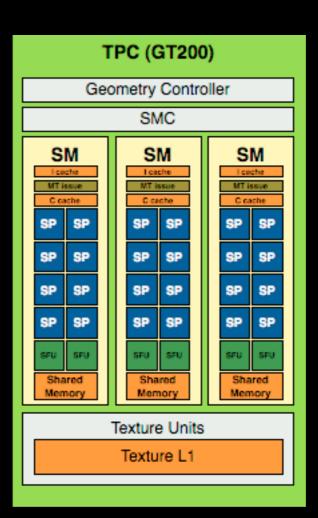




Array of 8 (eight) SPS

#### GPU Architecture (GT200)

#### Texture Processor Cluster 3 SM's

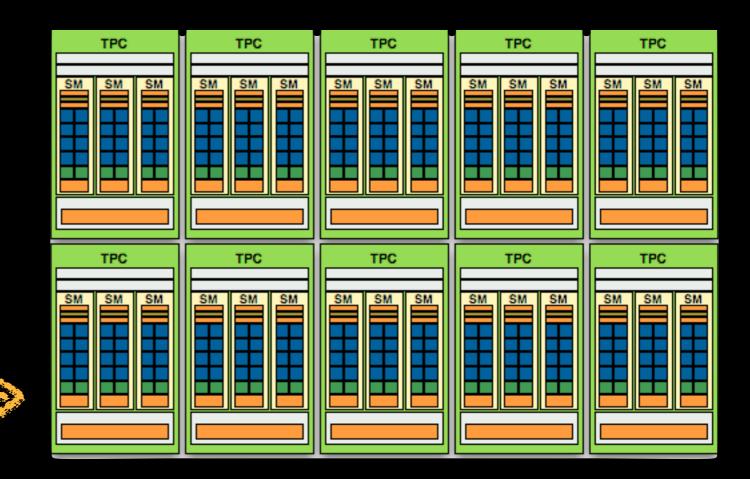


#### GPU Architecture (GT200)

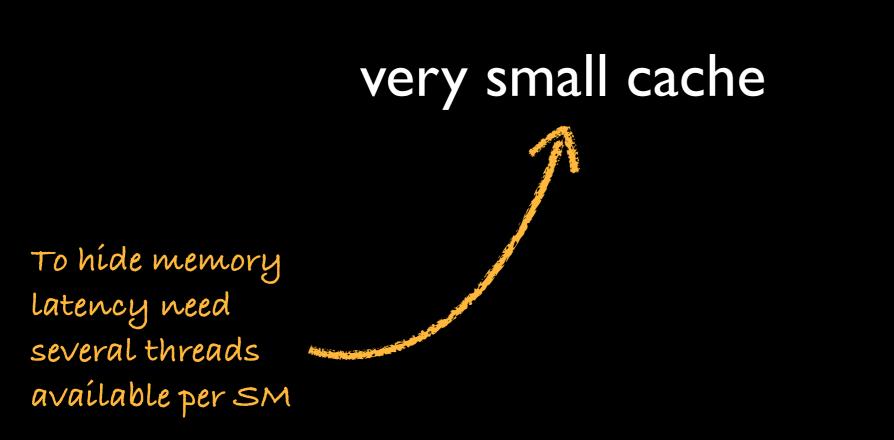
#### The beast

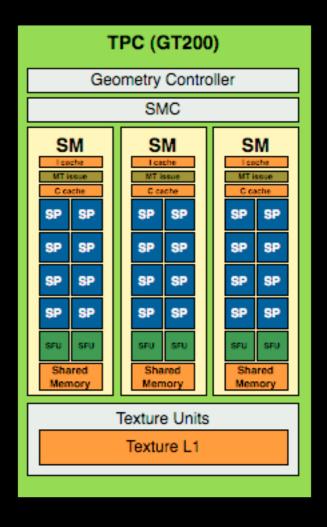
10 TPC'S 3 SM's per TPC 8 SP's per SM

Total of 240 SP's



#### GPU Architecture (GT200)



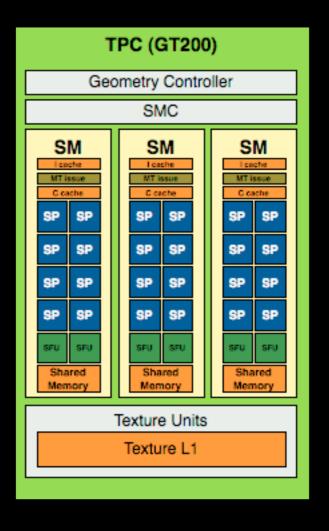


Schedule per group of 32 threads, called a warp

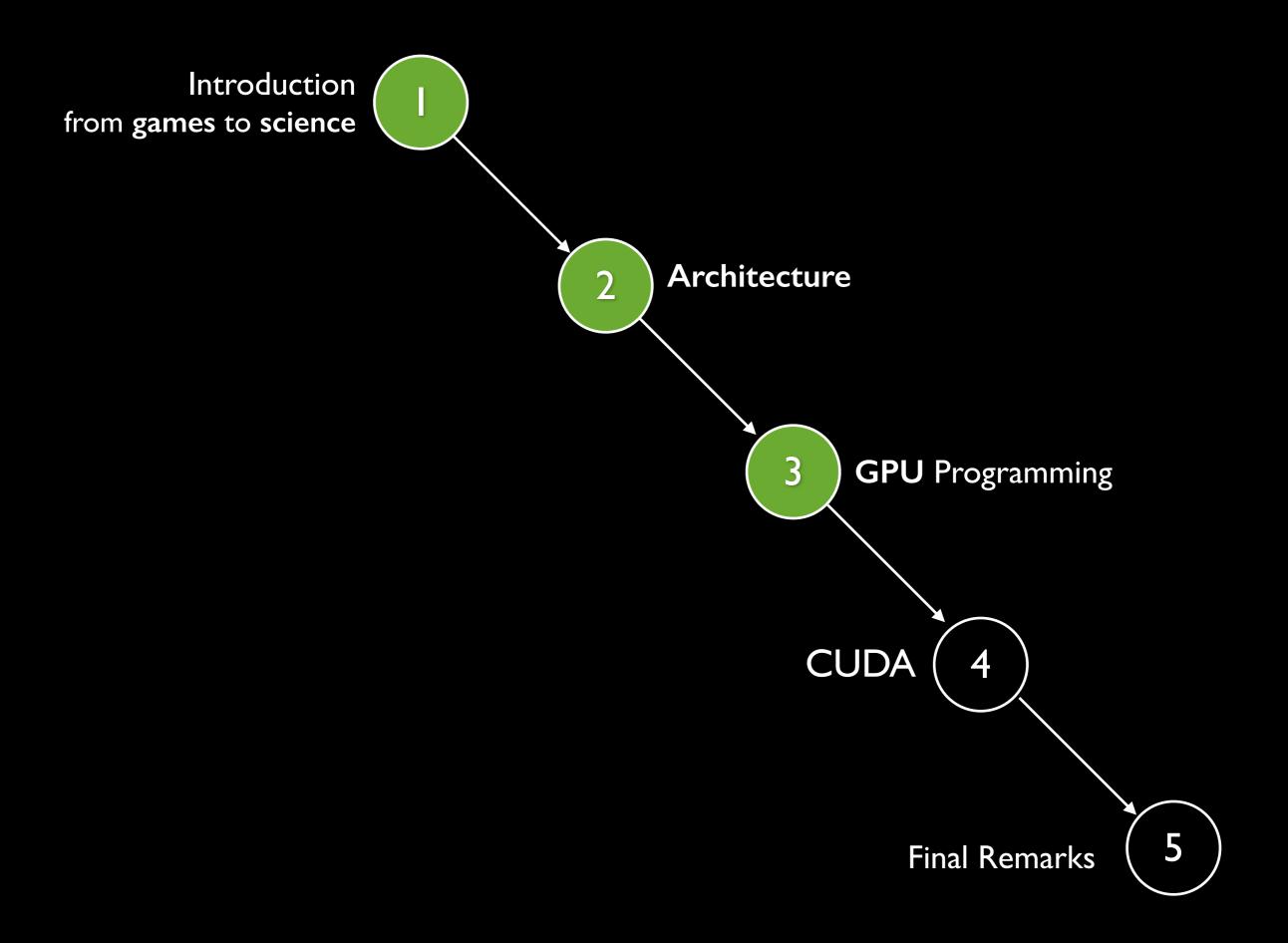
## GPU Architecture (GT200)

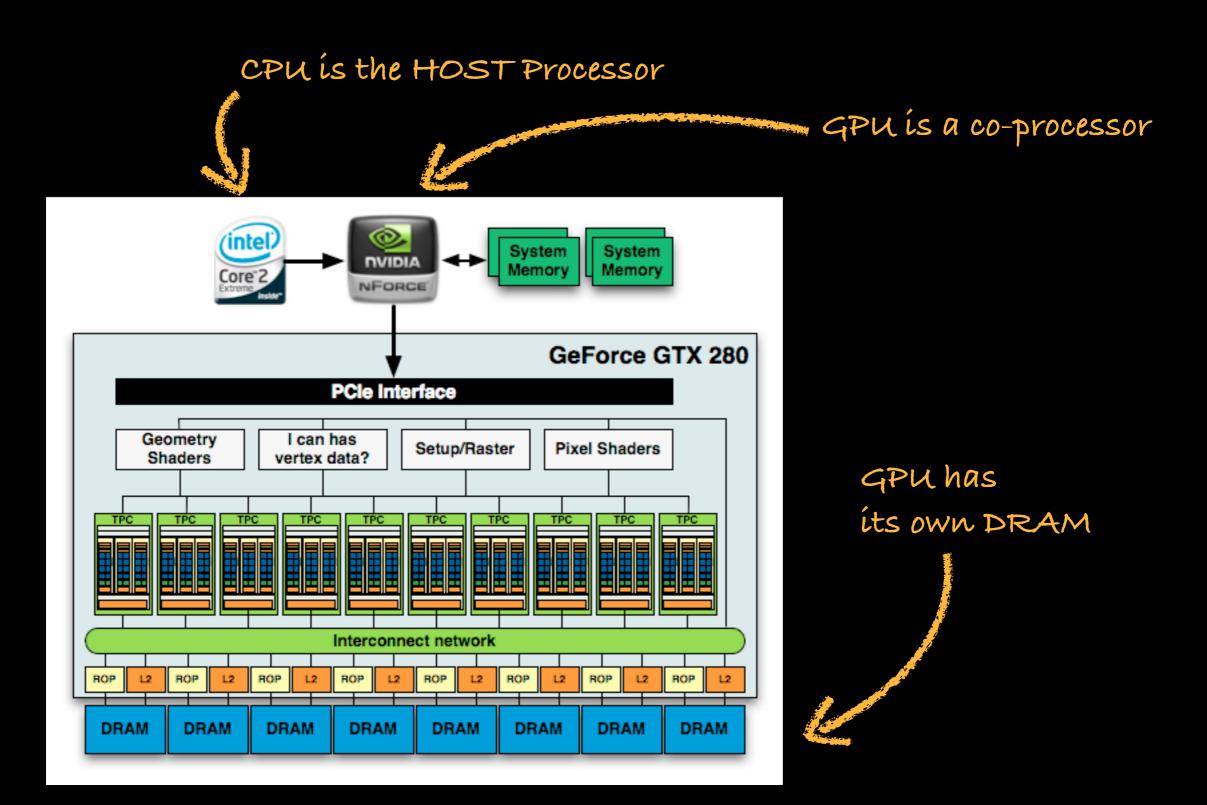
# Each SM handles 32 warps simultaneously

 $32 \times 32 = 1024$  threads per SM



## $1024 \times 30 = 30720$ simultaneous threads





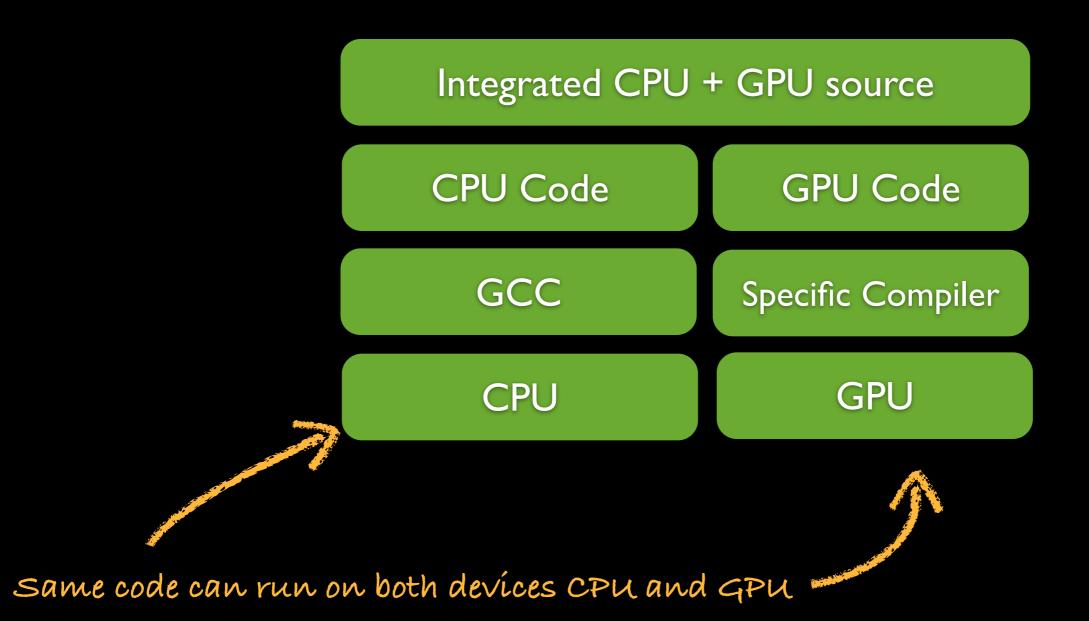
Massively parallel processor (GT200 - 30720 Threads)

- CPU send burst of threads to execute on the GPU

Use DMA to transfer from CPU DRAM to GPU DRAM

CPU becomes can do something useful aside with GPU

Applications must be rewritten to cope with GPU



Example I Discover your CUDA environment.

#### Using CUDA on Guane Step-by-step

Connect to guane

\$ ssh guane

Reserve a node on shared mode (so other users can have it too)

\$ oarsub -l nodes=1 -t timesharing -I

Download the CUDA exemples from <u>sc-camp.org</u>

\$ wget <u>http://www.sc-camp.org/cuda/gpu\_programming.tgz</u>

Configure the path to CUDA\_SDK

\$ export CUDA\_SDK\_PATH=/usr/local/cuda-6.5/

#### Using CUDA on Guane Step-by-step

Uncompress the folder

\$ tar zxvf gpu\_programming.tgz

Enter the directory

\$ cd gpu\_programming/01-devicequery

Compile

\$ make

Run

\$ ./device\_query

#### Using CUDA on Guane Step-by-step

All nodes have 8 GPU Tesla S2050

Yet no support to reserve a single CPU+GPU

DUDIA

ADDRESS !!

Share these GPUs wisely with your mates

Based on the idea of kernel

Essentially SPMD

Define single thread application code

Use thread id to assign different data per thread

Definition of a single thread computing function (or kernel)

## Definition of a single thread computing function (or kernel)

```
int kernel()
{
    int i = thread.id;
    a[i] = a[i] + b[i];
}
```

#### Definition of a single thread computing function (or kernel)



}

int kernel() int i = thread.id; a[i] = a[i] + b[i];

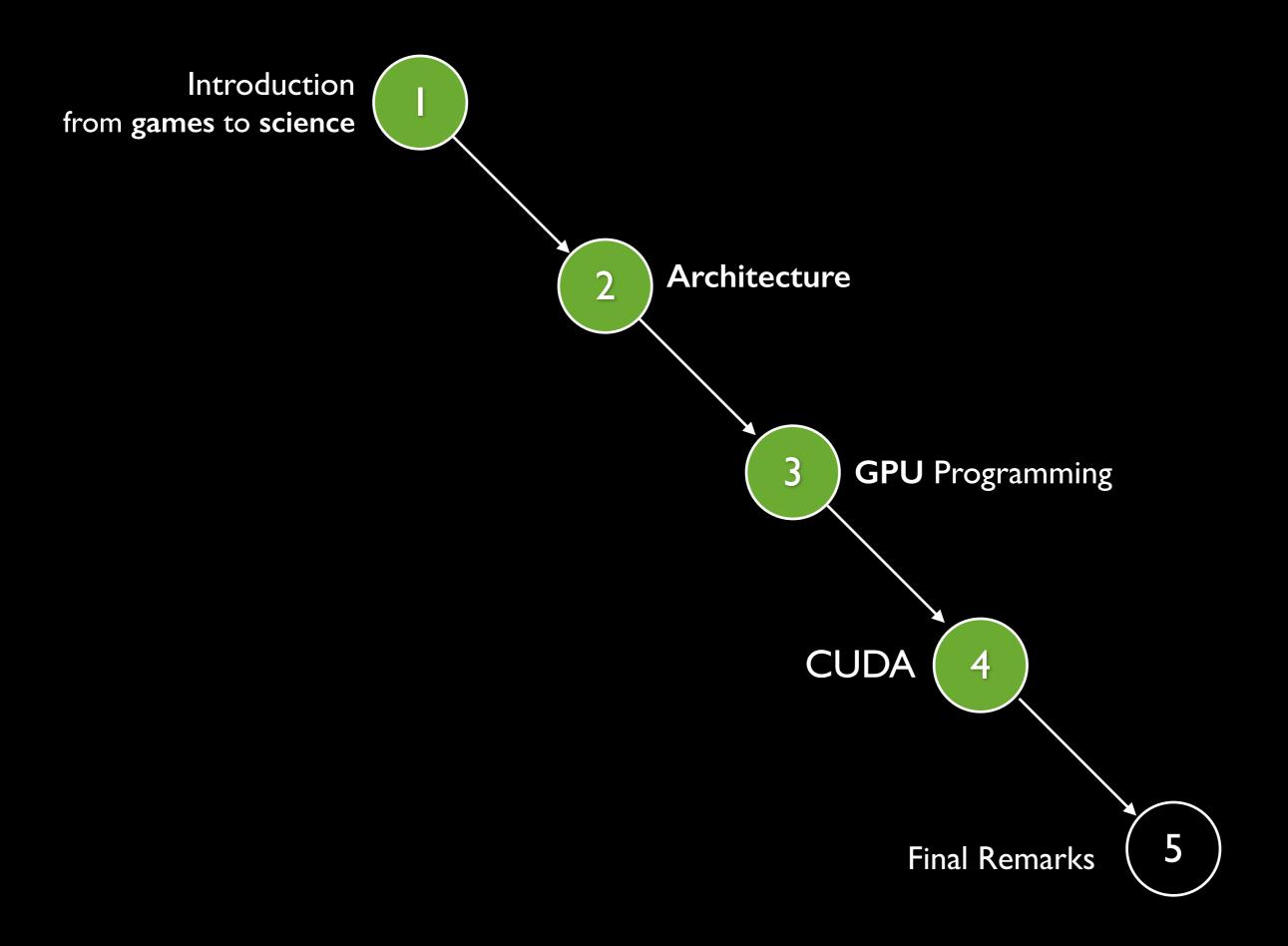
- 1- How to Compute the thread ID?
- 2- How do we copy data from CPU to GPU?
- 3- How to dispatch kernel on the device?
- 4- How to get results back when done?

Have support for operations on the Host (CPU) and Device (GPU)

Copy data from Host to Device
 Execute kernel on the device
 Wait for kernel to finish
 Copy data from Device to Host

mallocDeviceMemory copyFromHostToDevice computeKernel copyFromDeviceToHost

Depends on the programming interface



#### - C extension

- Support for several platforms:
  - Linux
  - Windows
  - MacOS
- Need to install NVIDIA Driver, Toolbox and SDK

#### Provide several libraries



#### STL C++ Port to CUDA



Linear Algebra cuBLAS

Requirements for Linux

- I NVIDIA CUDA aware card
- GCC installed
- Downloaded Toolkit, Driver, and SDK

MOSTRAR SITE

Step-by-step installation:

- Install the CUDA Toolkit
  \$ ./cudatoolkit\_4.2.9\_linux\_64\_ubuntul1.04.run
- Install the driver
  \$ sudo ./devdriver\_4.2\_linux\_64\_295.41.run
- Restart GUI
  \$ sudo /etc/init.d/gdm start
- Install SDK

\$./gpucomputingsdk\_4.2.9\_linux.run

Only the dríver requires superuser príviledges

#### Function directives

Kernel function must respect several properties must return void no static variables no recurrence no variable number of arguments		
	Execute on	Called from
device float DeviceFunc()	device	device
globalvoid kernelFunc()	device	host
<pre>host float HostFunc()</pre>	host	host

can be used combined with \_\_device\_\_

Example II Simple kernel hello world.

#### Hello World

```
__global__ void mykernel (void){
   //simple kernel does nothing
}
```

```
int main(void) {
    mykernel<<<1,1>>>();
    printf("Hello World!\n");
    return 0;
}
```

#### Single threaded application

```
int a[1024];
int b[1024];
int c[1024];
int main()
{
    for(int i=0; i<1024; i++){
        c[i] = a[i] + b[i];
    }
}
```

#### Single threaded application

```
int a[1024];
int b[1024];
int c[1024];
int main()
{
  for(int i=0; i<1024; i++){
    c[i] = a[i] + b[i];
  }
}
```

Where should we use parallel computing?

#### Single threaded application

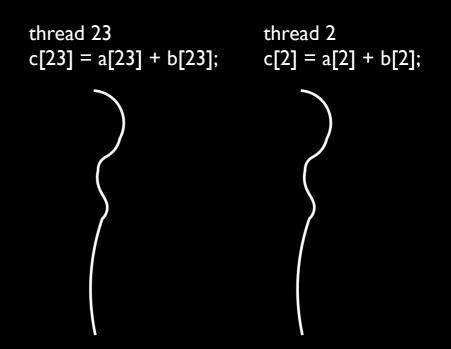
```
int a[1024];
int b[1024];
int c[1024];
int main()
{
   for(int i=0; i<1024; i++){
      c[i] = a[i] + b[i];
   }
}
```

#### Single threaded application

int a[1024]; int b[1024]; int c[1024]; int main() { for(int i=0; i<1024; i++){ c[i] = a[i] + b[i]; } }

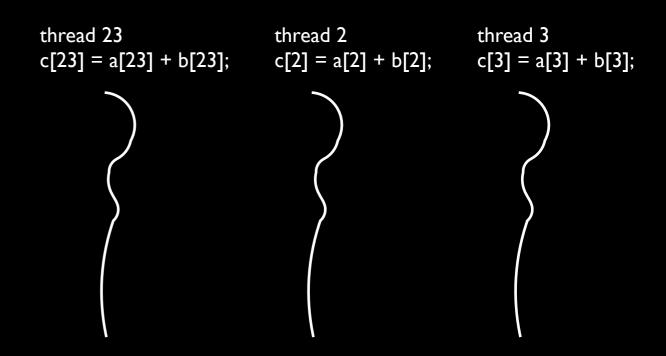
#### Single threaded application

int a[1024]; int b[1024]; int c[1024]; int main() { for(int i=0; i<1024; i++){ c[i] = a[i] + b[i]; } }



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int a[1024]; int b[1024]; int c[1024]; int main() { for(int i=0; i<1024; i++){ c[i] = a[i] + b[i]; } }



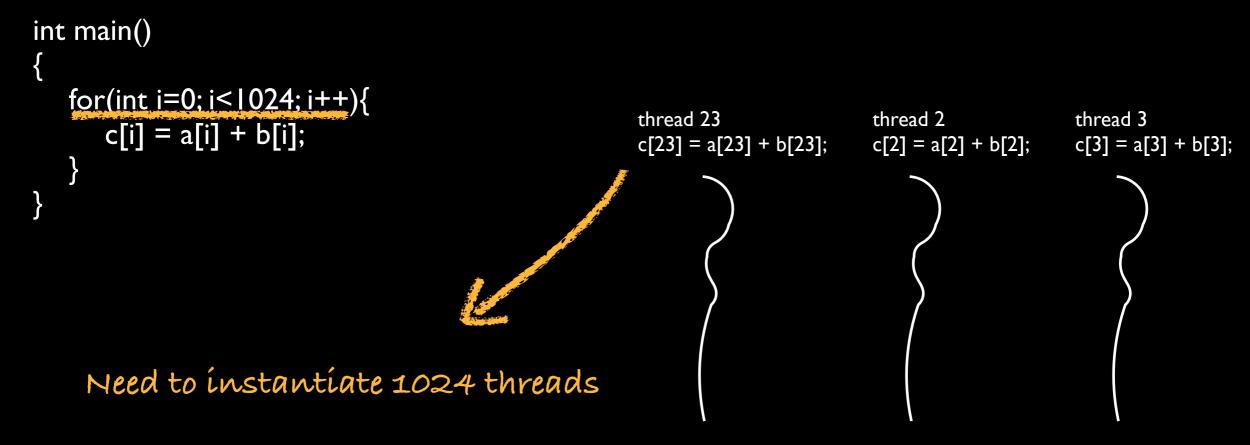
#### Single threaded application

int a[1024];

int b[1024];

int c[1024];

Multi threaded application



GT200 supports up to 30720 threads simultaneously!!!

Example III Add two integers. Adding two integers

\_\_global\_\_ void add(int \*a, int \*b, int \*c) {
 \*c = \*a + \*b;
}

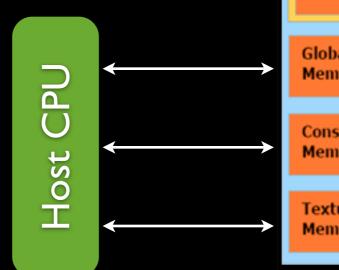
#### Adding two integers

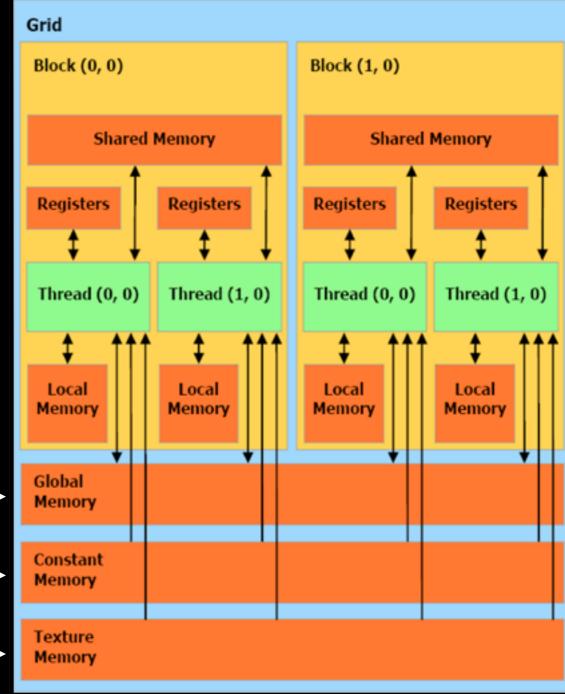
```
int main(void) {
     int a, b, c;
                                // host copies of a, b, c
     int *d_a, *d_b, *d_c;
                                // device copies of a, b, c
     int size = sizeof(int);
     // Allocate space for device copies of a, b, c
     cudaMalloc((void **)&d_a, size);
     cudaMalloc((void **)&d_b, size);
     cudaMalloc((void **)&d_c, size);
     // Setup input values
     a = 2;
     b = 7;
     // Copy inputs to device
     cudaMemcpy(d_a, &a, size, cudaMemcpyHostToDevice);
     cudaMemcpy(d_b, &b, size, cudaMemcpyHostToDevice);
     // Launch add() kernel on GPU
     add<<<1,1>>>(d_a, d_b, d_c);
     // Copy result back to host
     cudaMemcpy(&c, d_c, size, cudaMemcpyDeviceToHost);
     // Cleanup
     cudaFree(d_a); cudaFree(d_b); cudaFree(d_c);
     return 0;
 }
```

Memory allocation

```
cudaMalloc(...)
```

Allocate global memory 2 parameters: Pointer Number of bytes

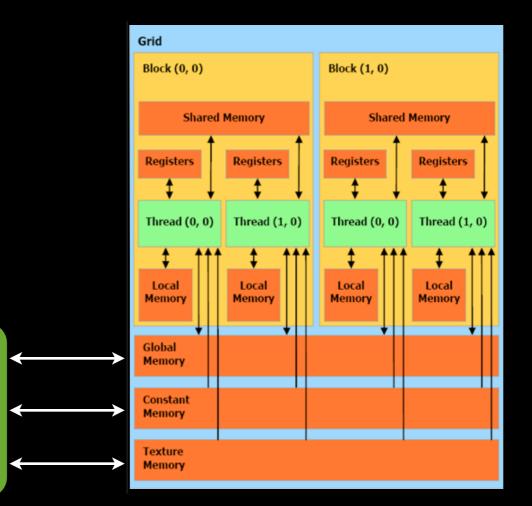




Transfer data

cudaMemcpy(...)

- 4 parameters: Destination pointer Source pointer Bytes to copy Transfer type
  - HostToHost HostToDevice DeviceToHost DeviceToDevice

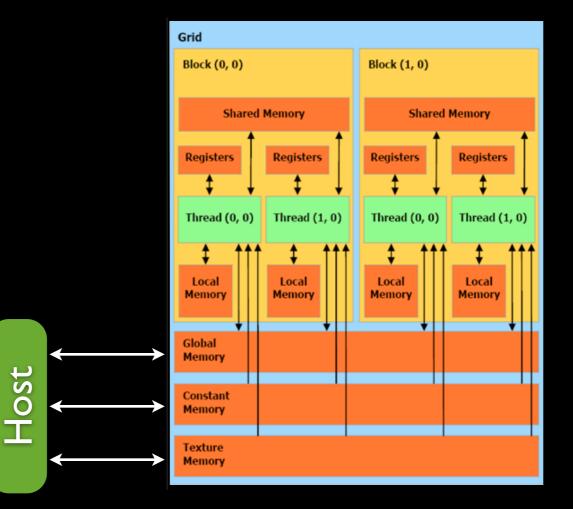


Host

Memory deallocation

cudaFree(...)

Frees global memory I parameter: Pointer



}

#### Simplified code

```
...
float *aHost, *bHost, *cHost;
...
global____void kernel(float *a, float *b, float *c){
    int i = threadidx.x;
    c[i] = a[i] + b[i];
}
```

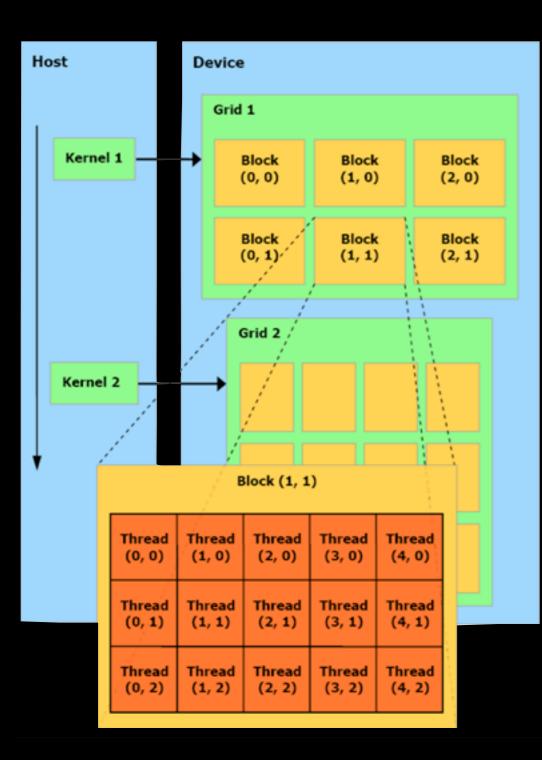
```
int main(){
   float *aDev, *bDev, *cDev;
```

cudaMalloc(void \*aDev, 512 \* sizeof(float)); cudaMemcpy(aDev, aHost, 512 \* sizeof(float));

cudaMalloc(void \*bDev, 512 \* sizeof(float)); cudaMemcpy(bDev, bHost, 512 \* sizeof(float));

```
kernel<<<1,512>>> (aDev, bDev, cDev);
```

cudaFree(aDev); cudaFree(bDev); cudaFree(cDev);



Thread indexing

Threads are organized in blocks

Blocks are organized in grids

Legacy from CG applications

### Grid

Block	Block	Block
(0,0)	(1,0)	(2,0)
Block	Block	Block
(0,1)	(I,I)	(2,1)
Block	Block	Block
(0,2)	(1,2)	(2,2)

### Grid

Block (0,0)	Block (1,0)	Block (2,0)	Bloc	ck		
Block	Block	Block	Thread	Thread	Thread	Thread
(0,1)	(1,1)	(2,1)	(0,0)	(1,0)	(2,0)	(3,0)
Block	Block	Block	Thread	Thread	Thread	Thread
(0,2)	(1,2)	(2,2)	(0,1)	(1,1)	(2,1)	(3,1)
			Thread (0,2)	Thread (1,2)	Thread (2,2)	Thread (3,2)

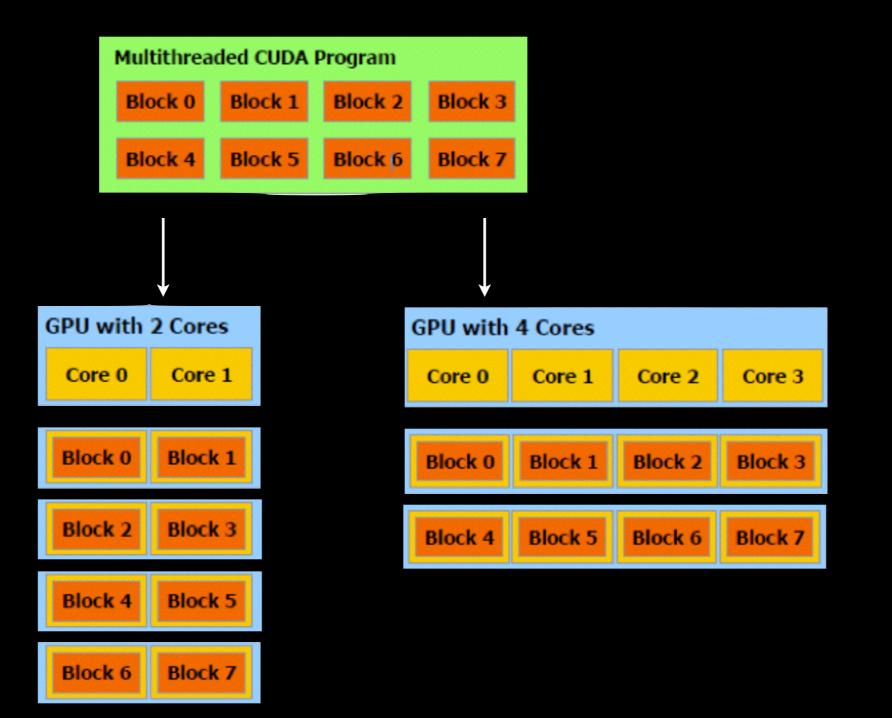
#### mapping threads

Block	Thread	Thread	Thread	Thread
	(0,0)	(1,0)	(0,0)	(1,0)
(0,0)	Thread	Thread	Thread	Thread
	(0,1)	(I,I)	(0,1)	(I,I)
Block	Thread	Thread	Thread	Thread
	(0,0)	(1,0)	(0,0)	(1,0)
(0,I)	Thread	Thread	Thread	Thread
	(0,1)	(1,1)	(0,1)	(1,1)

Block (1,0)

Block (I,I)

dim3 Grid(2,2); dim3 Block(2,2); kernel<<<Grid,Block>>>(parameters);



#### How can we arrange 6 threads?

### Block (0,0)

Thread (0,0)	Thread (1,0)			Thread (5,0)
		(_, _ ,		

MAX THREADS PER BLOCK DEPEND ON THE ARCHITECTURE



#### How can we arrange 6 threads?

Block (0,0)

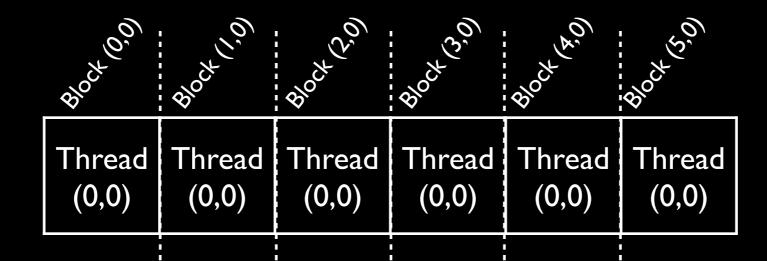
Thread	Thread	Thread	Thread	Thread	Thread
(0,0)	(1,0)	(2,0)	(3,0)	(4,0)	(5,0)

Block (0,0)			Blc	ock (I	,0)
Thread	Thread	Thread		Thread	Thread
(0,0)	(1,0)	(2,0)		(1,0)	(2,0)

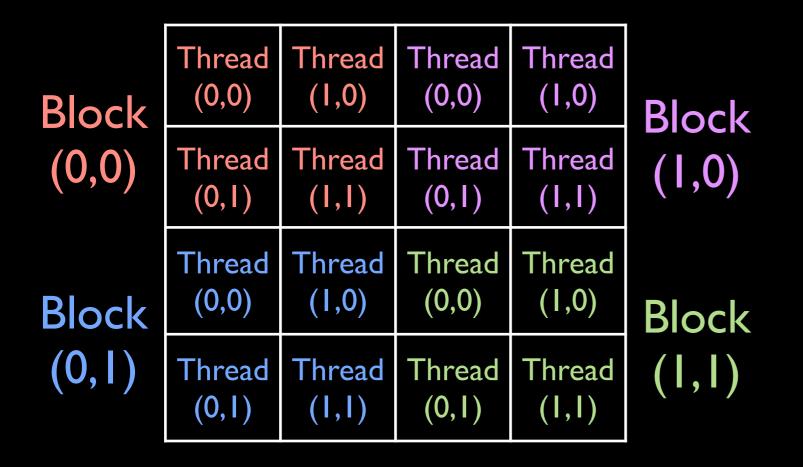
How can we arrange 6 threads?

Block (0,0)		Block (1,0)		Block (2,0)	
Thread (0,0)	Thread (1,0)	Thread (0,0)	Thread (1,0)	Thread (0,0)	Thread (1,0)

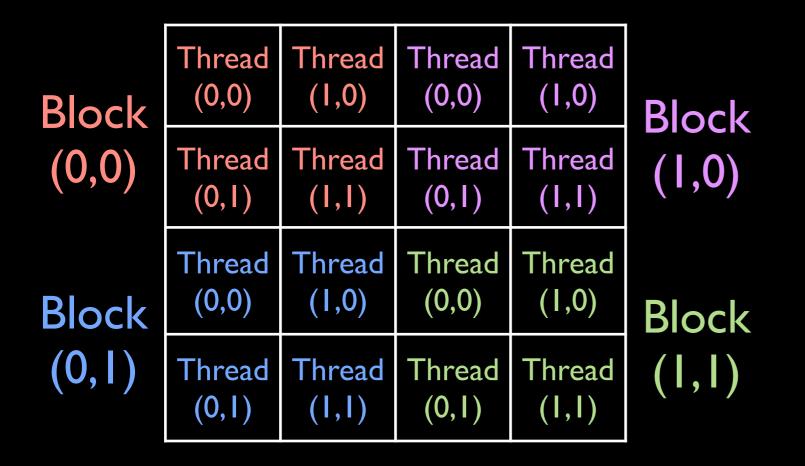
How can we arrange 6 threads?



#### Mapping on an unique grid



#### Mapping on an unique grid



idx = blockIdx.x\*blockDim.x + threadIdx.x;

idy = blockIdx.y\*blockDim.y + threadIdx.y;

#### Mapping on an unique grid

Block	Thread (0,0)	Thread (1,0)	Thread (0,0)	Thread (1,0)	Block				
(0,0)	Thread (0,1)	Thread (1,1)	Thread (0,1)	Thread (1,1)	(1,0)	Thread (0,0)	Thread (1,0)	Thread (2,0)	Thread (3,0)
Block	Thread (0,0)	Thread (1,0)	Thread (0,0)	Thread (1,0)	Block	(0,0) Thread (0,1)		(2,0) Thread (2,1)	
(0,1)	Thread (0,1)	Thread (1,1)	Thread (0,1)	Thread (1,1)	( , , , , )	Thread	Thread	Thread	Thread
						(0,2)	(1,2)	(2,2)	(3,2)

Thread

(1,3)

Thread

(3,3)

Thread

(2,3)

Thread

(0,3)

idx = blockldx.x\*blockDim.x + threadldx.x;

idy = blockIdx.y\*blockDim.y + threadIdx.y;

#### Get an unique thread index

Thread	Thread	Thread	Thread
(0,0)	(1,0)	(2,0)	(3,0)
Thread	Thread	Thread	Thread
(0,1)	(I,I)	(2,1)	(3,1)
Thread	Thread	Thread	Thread
(0,2)	(1,2)	(2,2)	(3,2)
Thread	Thread	Thread	Thread
(0,3)	(1,3)	(2,3)	(3,3)

k = idx + idy\*blockDim.x\*gridDim.x;

#### Get an unique thread index

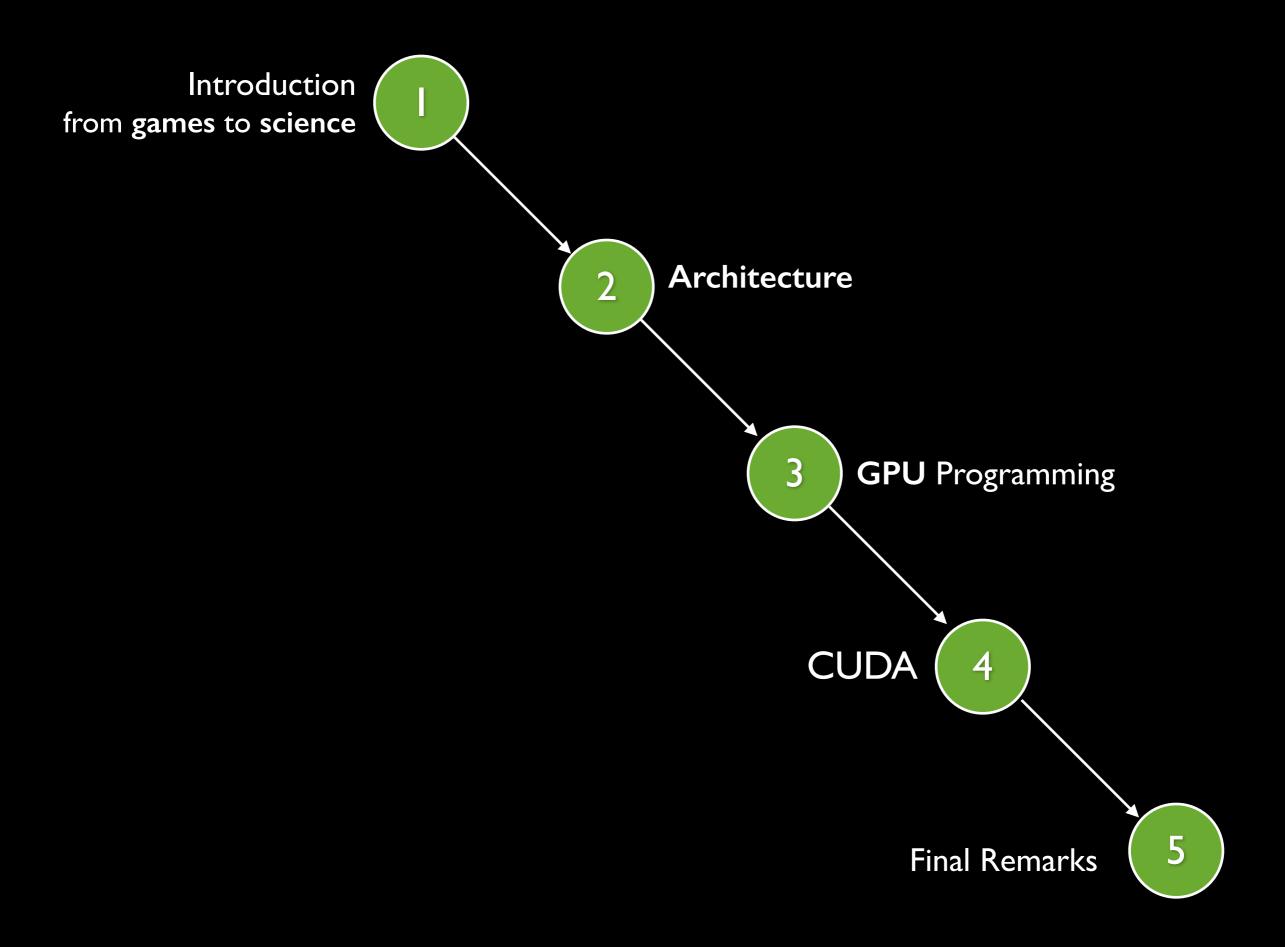
Thread	Thread	Thread	Thread
(0,0)	(1,0)	(2,0)	(3,0)
Thread	Thread	Thread	Thread
(0,1)	(I,I)	(2,1)	(3,1)
Thread	Thread	Thread	Thread
(0,2)	(1,2)	(2,2)	(3,2)
Thread	Thread	Thread	Thread
(0,3)	(1,3)	(2,3)	(3,3)



Thread	Thread	Thread	Thread
(0)	(I)	(2)	(3)
Thread	Thread	Thread	Thread
(4)	(5)	(6)	(7)
Thread	Thread	Thread	Thread
(8)	(9)	(10)	(11)
Thread	Thread	Thread	Thread
(12)	(13)	(14)	(15)

k = idx + idy\*blockDim.x\*gridDim.x;

Exercise Implementing the sum of two vectors using CUDA of a unlimited number of elements.



# **CUDA** Programming

SDK has many applications:

\$ cd \$NVIDIA\_CUDA\_SDK

\$ make

\$ make check

\$ C/bin/linux/release/

### GPU is good for...

loosely coupled threads (avoid synchronisation)

computing bound applications

these architectures can not replace general purpose CPU

great insight for future architectures

#### **CUDA** Pros

### **CUDA** Cons

Support for several OS

A lot of documentation

Many libraries available

Great performance

**NVIDIA** proprietary

## Architectures of Today

#### Highly heterogeneous



## Architectures of Today

#### Highly heterogeneous

#### NVIA Tegra ARM + GPU



### Architectures of Today

#### Highly heterogeneous

#### Intel Xeon Phi

" Moving a code to Intel Xeon Phi might involve sitting down and adding a couple lines of directives that takes a few minutes. Moving a code to a GPU is a project."

Dan Stanzione, Deputy Director at Texas Advanced Computing Center



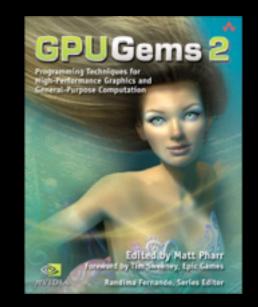
The Intel® Xeon® Phí™ Coprocessor: Parallel Processing, Unparalleled Discovery

From intel's website

# Further help

CUDA Developer Network

http://developer.download.nvidia.com/compute/cuda/4\_1/rel/toolkit/docs/online/ group\_\_CUDART\_\_MEMORY\_g48efa06b81cc031b2aa6fdc2e9930741.html



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#### GPU Gems 2, available online

#### <u>http://http.developer.nvidia.com/GPUGems2/</u> gpugems2\_part01.html

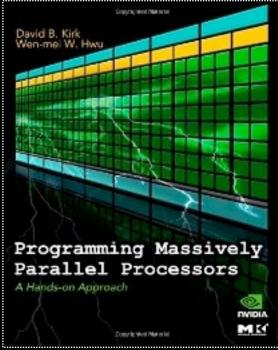


GPU Gems 3, available online

<u>https://developer.nvidia.com/gpugems/GPUGems3/</u> gpugems3\_pref01.html

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Programming Massively Parallel Processors: A Hands-on Approach, David B. Kirk and Wen-Mei Hwu, Second Edition, Morgan Kaufmann, 2009



NVIDIA developer zone, <u>http://developer.nvidia.com/</u>

Exercise IV Naïve matrix multiplication on GPU.

http://www.es.ele.tue.nl/~mwijtvliet/5KK73/?page=mmcuda